UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/696,366	10/25/2000	Randal N. Linden	1005/203	3221

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LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/696,366	LINDEN, RANDAL N.
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is

  closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4 and 6-19* is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4* is/are allowed.

6)☒ Claim(s) *1 and 6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☐ All b)☐ Some * c)☐ None of:

  1.☐ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage

  application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 04/12/2004.

Claims 2, 3, and 5 have been cancelled. Claims 8-19 are newly added. Claims 1, 4,

and 6-19 are pending now in the Action.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1, 6-9, and 10-19 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Blasciak, Andrew, US patent no. 5,103,394 in view of Dean Klein, US

patent no. 6,047,381.

As per claim 1, Blasciak discloses a method and system for emulating speed

execution of program instruction codes designed for a target system in a host with

feature limitations substantially similar to the claimed invention (Abstract and Summary

of the Invention).   According to Blasciak, the emulation method includes steps of

Measuring or calculating an execution speed of the target system in execution of

the program instructions and a host system in emulation of target program (col. 4, lines

3-57, col. 5, lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18),

Determining an execution speed of the host system used in the speed execution

emulation, thus, it would be easy to derive a speed variance (difference) between the

host processor and the target processor under emulated (Fig. 12, col. 10, lines 25-40,

col. 11, line 52 to col. 12, line 54, col. 16, lines 49-66, and cols. 13-18 for details

description of target execution speed measurement), and configuring or reconfiguring

the host system in order to conform to the execution speed of the target system in

execution of the target program (cols. 12-18) for emulation or debugging process. In

other words, this process is required to adjust to measurement of speed change

(Background of the Invention, col. 18, lines 32-54, for exemplary). (see Klein below for

calculation of speed difference between the host and target program (codes) execution

speed). Blasciak does not expressly disclose dynamically adjusting the execution

speed of the host system by dynamically increasing the host execution speed when the

host execution speed is less than the target execution speed, and dynamically

decreasing the host execution speed when the host execution speed is greater than the

target execution speed as claimed.   Such claimed feature is well known in the art. In

fact, Klein teaches a method and system of clock speed adjustment logic (col. 6, lines

51-67) for dynamically adjusting execution speed of a host system based on speed

change (or variant) whence execution of a series of target instructions for a target

system with target execution speed variant as required by hardwares, codes, or

compatibility constraints (col. 4, lines 13-55). Klein dynamic adjustment of execution

speed of the host system is to maintain software compatibility to hardware emulation

(col. 2, lines 1-37) and for Blasciak real time code emulation and measurement as disclosed in col. 14, lines 12-55.

With these motivations, it would have been obvious for practitioner in the art at the time of the invention was made to combine Klein teaching of execution speed adjustment to target execution speed of the host system by using the speed adjusting logic as above into the target emulation system in Blasciak to adjust and change host speed execution during emulation of the target system.

As per claim 6, Klein teaches clock speed adjustment based on predetermined acceptance speed execution change or variance between the host and target system and dynamic adjusting host execution speed to maintain software compatibility to hardware constraint requirements (col. 4, lines 13-55, for example).

As per claim 7, Blasciak discloses execution speed change(s) or variance. Such speed change or variation is due to instruction execution requirements. It requires speed comparison or speed ratio to determine speed variant or execution speed change.

As per claim 8, Blasciak discloses speed execution and time required to execute a predetermined number of instructions by the target system (col. 4, lines 3-57, col. 5, lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18), and an amount of time used by the host system, of course to emulate execution of a particular block of instructions containing the predetermined number of instructions (col. 10, lines 49-6, col. 11, line 52 to col. 12, line 54, col. 14, line 57 to col. 15, line 19, for example). Klein also teaches such feature in clock speed adjustment logic to change execution speed of the

host system to adapt to system constraints and code compatibility (col. 3, lines 29-37,

col. 4, lines 28-37, col. 5, lines 8-18, and col. 6, lines 50-67).

As per claim 9, Klein teaches clock speed adjustment based on speed variance

or changes due to execution speed requirements (col. 4, lines 13-55, col. 6, lines 51-

67). With the reasons as set forth, this would be obvious for those skilled in the art at

the time of the invention was made to combine clock speed adjustment logic as taught

in Klein into the Blasciak to adjust execution speed of the host system in measurement

of target system performance.

As per claim 10, Blasciak discloses a method and system including a machine-

readable medium having information recorded thereon for emulating execution of

program instruction codes designed for a target system in a host with feature limitations

substantially similar to the claimed invention (Abstract and Summary of the Invention).

According to Blasciak, the emulation method includes steps of

Calculating an execution speed of the target system in execution of the program

instructions and a host system in emulation of target program (col. 4, lines 3-57, col. 5,

lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18),

Determining an execution speed of the host system used in the speed execution

emulation, thus, it would be easy to derive a speed variance (difference) between the

host processor and the target processor under emulated (Fig. 12, col. 10, lines 25-40,

col. 11, line 52 to col. 12, line 54, col. 16, lines 49-66, and cols. 13-18 for details

description of target execution speed measurement), and configuring or reconfiguring

the host system in order to conform to the execution speed of the target system in

execution of the target program (cols. 12-18) for emulation or debugging process. In other words, this process is required to adjust to measurement of speed change (Background of the Invention, col. 18, lines 32-54, for exemplary). Blasciak does not expressly disclose dynamically adjusting the execution speed of the host system by dynamically increasing the host execution speed when the host execution speed is less than the target execution speed, and dynamically decreasing the host execution speed when the host execution speed is greater than the target execution speed as claimed. Such claimed feature is well known in the art. In fact, Klein teaches a method and system of clock speed adjustment logic (col. 6, lines 51-67) for dynamically adjusting execution speed of a host system based on speed change (or variant) whence execution of a series of target instructions for a target system with target execution speed variant as required by hardwares, codes, or compatibility constraints (col. 4, lines 13-55). Klein dynamic adjustment of execution speed of the host system is to maintain software compatibility to hardware emulation (col. 2, lines 1-37).

It would have been obvious for practitioner in the art at the time of the invention was made to combine Klein teaching of execution speed adjustment to target execution speed of the host system by using the speed adjusting logic as above into the target emulation system in Blasciak to adjust and change host speed execution during emulation of the target system.

As per claim 11, Klein teaches clock speed adjustment based on predetermined acceptance speed execution change or variance between the host and target system

and dynamic adjusting host execution speed to maintain software compatibility to

hardware constraint requirements (col. 4, lines 13-55, for example).

As per claim 12, Blasciak discloses execution speed changes or variance. Such

speed change or variation is due to instruction execution requirements. Thus, it would

require speed comparison such as speed ratio, relative speed, or difference to

determine speed variant or execution speed change.

As per claim 13, Blasciak discloses speed execution and time required to

execute a predetermined number of instructions by the target system (col. 4, lines 3-57,

col. 5, lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18), and an amount

of time used by the host system to emulate execution of a particular block of instructions

containing the predetermined number of instructions (col. 10, lines 49-6, col. 11, line 52

to col. 12, line 54, col. 14, line 57 to col. 15, line 19, for example) in determination of

code execution measurement in real time. Klein also teaches such feature in clock

speed adjustment logic to change execution speed of the host system to adapt to

system constraints and code compatibility (col. 3, lines 29-37, col. 4, lines 28-37, col. 5,

lines 8-18, and col. 6, lines 50-67).

As per claim 14, with the motivation as set above, it would have been obvious for

practitioner in the art at the time of the invention was made to combine Klein teaching of

clock speed adjustment logic (col. 6, lines 51-67) for dynamically adjusting execution

speed of a host system based on speed change (or variant) whence execution of a

series of target instructions for a target system with target execution speed variant as

required by hardwares, codes, or compatibility constraints (col. 4, lines 13-55). Klein

dynamic adjustment of execution speed of the host system is to maintain software

compatibility to hardware emulation (col. 2, lines 1-37) into the target emulation system

in Blasciak to adjust and change host speed execution during emulation of the target

system in real time program execution and real time measurement.

As per claim 15, Blasciak discloses a method and system for emulating speed

execution of program instruction codes designed for a target system in a host with

feature limitations substantially similar to the claimed invention (Abstract and Summary

of the Invention).   According to Blasciak, the emulation system includes means for

performing steps:

Measuring or calculating an execution speed of the target system in execution of

the program instructions and a host system in emulation of target program (col. 4, lines

3-57, col. 5, lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18),

Determining an execution speed of the host system used in the speed execution

emulation, thus, it would be easy to derive a speed variance (difference) between the

host processor and the target processor under emulated (Fig. 12, col. 10, lines 25-40,

col. 11, line 52 to col. 12, line 54, col. 16, lines 49-66, and cols. 13-18 for details

description of target execution speed measurement), and configuring or reconfiguring

the host system in order to conform to the execution speed of the target system in

execution of the target program (cols. 12-18) for emulation or debugging process. In

other words, this process is required to adjust to measurement of speed change

(Background of the Invention, col. 18, lines 32-54, for exemplary). (see Klein below for

calculation of speed difference between the host and target program (codes) execution

speed). Blasciak does not expressly disclose dynamically adjusting the execution speed of the host system by dynamically increasing the host execution speed when the host execution speed is less than the target execution speed, and dynamically decreasing the host execution speed when the host execution speed is greater than the target execution speed as claimed. Such claimed feature is well known in the art. In fact, Klein teaches a method and system of clock speed adjustment logic (col. 6, lines 51-67) for dynamically adjusting execution speed of a host system based on speed change (or variant) whence execution of a series of target instructions for a target system with target execution speed variant as required by hardwares, codes, or compatibility constraints (col. 4, lines 13-55). Klein dynamic adjustment of execution speed of the host system is to maintain software compatibility to hardware emulation (col. 2, lines 1-37) and for Blasciak real time code emulation and measurement as disclosed in col. 14, line12-55.

With these motivations, it would have been obvious for practitioner in the art at the time of the invention was made to combine Klein teaching of execution speed adjustment to target execution speed of the host system by using the speed adjusting logic as above into the target emulation system in Blasciak to adjust and change host speed execution during emulation of the target system.

As per claim 16, Klein teaches clock speed adjustment based on predetermined acceptance speed execution change or variance between the host and target system and dynamic adjusting host execution speed to maintain software compatibility to

hardware constraint requirements (col. 4, lines 13-55, for example) and to adapt speed change in real time program execution and code measurement.

As per claim 17, Blasciak discloses execution speed changes or variance. Such speed change or variation is due to instruction execution requirements. It requires speed comparison or speed ratio to determine speed variant or execution speed change.

As per claim 18, Blasciak and Klein discloses speed execution and time required to execute a predetermined number of instructions by the target system (col. 4, lines 3-57, col. 5, lines 20-35, Figs. 12, 13, col. 10, lines 10-66, col. 17, lines 1-18), and an amount of time used by the host system to emulate execution of a particular block of instructions containing the predetermined number of instructions (col. 10, lines 49-6, col. 11, line 52 to col. 12, line 54, col. 14, line 57 to col. 15, line 19, for example) adaptively to real time measurement. Klein also teaches such feature in clock speed adjustment logic to change execution speed of the host system to adapt to system constraints and code compatibility (col. 3, lines 29-37, col. 4, lines 28-37, col. 5, lines 8-18, and col. 6, lines 50-67).

As per claim 19, Klein teaches clock speed adjustment based on speed variance or changes due to execution speed requirements (col. 4, lines 13-55, col. 6, lines 51-67). With the reasons as set forth, this would be obvious for those skilled in the art at the time of the invention was made to combine clock speed adjustment logic as taught in Klein into the Blasciak to adjust execution speed of the host system in measurement of target system performance.

Allowable Subject Matter

1.   Claim 4 is allowed. The following is a statement of reasons for the indication of allowable subject matter:

2.   Claim 4 requires the distinct features of by selecting a reference determined by an arbitrary time quantum of the execution speed, tracking the instruction cycles executed, determining an elapsed time period by querying a timing source, and determining a timing reference by comparing the elapsed time with the time quantum. The prior art of record does not show such distinct features as claimed to simulate the operating speed of the target system.   Claim 4 is deemed allowable.

Response to Arguments

1.   Applicant's arguments with respect to amended claims 1, 6-9, and 10-19 have been considered but are moot in view of the new ground(s) of rejection.

2.   In response to applicant's argument Blasciak does not expressly disclose the amended feature of dynamically adjusting speed execution of the host system accordingly to speed execution of the target program under emulation by the host (page 9, last paragraph), the examiner responds this argued feature is not explicitly disclose in Blasciak. Such feature is however well known in the data processing and software simulation art.   Klein teaches a method and system of clock speed adjustment logic (col. 6, lines 51-67) for dynamically adjusting execution speed of a host system based on speed change (or variant) whence execution of a series of target instructions for a target system with target execution speed variant as required by hardwares, codes, or compatibility constraints (col. 4, lines 13-55). Klein dynamic adjustment of execution

speed of the host system is to maintain software compatibility to hardware emulation (col. 2, lines 1-37) and for Blasciak real time code emulation and measurement as disclosed in col. 14, line12-55.

With these motivations, it would have been obvious for practitioner in the art at the time of the invention was made to combine Klein teaching of execution speed adjustment to target execution speed of the host system by using the speed adjusting logic as above into the target emulation system in Blasciak to adjust and change host speed execution during emulation of the target system.

Conclusion

1.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

2.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 08, 2004

Thai Phan

Patent Examiner